Claims:

1. An image-reject mixer comprising:

a first mixing branch having a first plurality of mixers, each of said first plurality of mixers having a local oscillator (LO) input;

a second mixing branch having a second plurality mixers, each of said second plurality of mixers having a LO input;

a combiner for generating an intermediate frequency (IF) signal from the outputs of said first and second mixing branches; and

commutating circuitry for commutating said LO inputs of each of said first plurality of mixers and each of said second plurality of mixers between in-phase and quadrature phases, and for commutating the outputs of said first and second mixing branches between each other.

2. The image-reject mixer of claim 1 wherein said commutating circuitry generates two complementary 50% duty cycle clock signals for commutating said LO inputs of each of said first plurality of mixers and each of said second plurality of mixers between in-phase and quadrature phases, and for commutating said first and second branches between each other.

3. The image-reject mixer of claim 2 wherein said clock signals are waveforms selected from the group consisting of square waves and pseudo-random digital signals.

4. The image-reject mixer of claim 2 wherein said commutating circuitry commutates the outputs of said first and second mixing branches between each

other by modulating the output of said combiner by the difference between said clock signals.

5. The image-reject mixer of claim 1 wherein said commutating circuitry couples a LO signal that is commutated between in-phase and quadrature phase to said LO inputs of each of said first plurality of mixers and each of said second plurality of mixers.

6. The image-reject mixer of claim 1 wherein said combiner comprises an adder and a subtractor for generating two IF signals corresponding to two RF signals that are images of each other.

7. An image-reject mixer comprising:

a first mixing branch having a first plurality of mixers;

a second mixing branch having a second plurality mixers;

a combiner for generating an intermediate frequency (IF) signal from the outputs of said first and second mixing branches; and

commutating circuitry for commutating each of said first plurality of mixers and each of said second plurality of mixers between each other, and for commutating the outputs of said first and second branches between each other.

8. The image-reject mixer of claim 7 wherein said commutating circuitry generates two complementary 50% duty cycle clock signals for commutating said LO inputs of each of said first plurality of mixers and each of said second plurality of mixers between each other, and for commutating said first and second branches between each other.

9. The image-reject mixer of claim 8 wherein said clock signals are waveforms selected from the group consisting of square waves and pseudo-random digital signals.

10. The image-reject mixer of claim 8 wherein said commutating circuitry commutates the outputs of said first and second mixing branches between each other by modulating the output of said combiner by the difference between said clock signals.

11. The image-reject mixer of claim 7 wherein said combiner comprises an adder and a subtractor for generating two IF signals corresponding to two RF signals that are images of each other.

12. An image-reject mixer comprising

a first mixer having a first filter and a local oscillator (LO) input;

a second mixer having a second filter and a LO input; and

commutating circuitry for commutating said LO inputs of said first mixer and said second mixer between in-phase and quadrature phases.

13. The image-reject mixer of claim 12 wherein said commutating circuitry generates two complementary 50% duty cycle clock signals for commutating said LO inputs of said first mixer and said second mixer between in-phase and quadrature phases.

14. The image-reject mixer of claim 13 wherein said clock signals are waveforms selected from the group consisting of square waves and pseudo-random digital signals.

15. The image-reject mixer of claim 12 wherein said commutating circuitry couples a LO signal that is commutated between in-phase and quadrature phases to said LO inputs of said first mixer and said second mixer.

16. The image-reject mixer of claim 12 further comprising a commutating mixer for modulating the output of said second filter by the difference between said complementary clock signals, said commutating mixer having a third filter.

17. A method of rejecting an image signal comprising:

mixing a radio frequency (RF) signal with a first local oscillation (LO) signal to generate a first intermediate frequency (IF) signal;

mixing said first IF signal with a second LO signal to generate a second IF signal; and

commutating said first and second LO signals between in-phase and quadrature phases.

18. The method of claim 17 wherein said commutating step comprises:

generating two complementary 50% duty cycle clock signals; and

commutating said first and second LO signals between in-phase and quadrature phases in accordance with said clock signals.

19. The method of claim 18 wherein said clock signals are waveforms selected from the group consisting of square waves and pseudo-random digital signals.

20. The method of claim 18 further comprising modulating said second IF signal by the difference between said clock signals.